

WHAT IS CLAIMED IS:

1 1. Circuitry for controlling the oscillating frequency of an
2 oscillator, the circuitry comprising:

3 a plurality of capacitors, each of which is independently
4 selectable by a control signal, and each of which provides a
5 controllable amount of capacitance to the oscillator to
6 control the oscillating frequency of the oscillator.

1 2. The circuitry of claim 1, wherein each of the plurality
2 of capacitors has a different capacitance than the other
3 capacitors, and a predefined amount of capacitance is provided
4 by a predetermined combination of capacitors.

1 3. The circuitry of claim 2, wherein the capacitors are
2 drain-source connected MOSFETs.

1 4. The circuitry of claim 3, wherein the MOSFETs are P-type
2 enhancement mode MOSFETs.

1 5. The circuitry of claim 3, wherein the MOSFETs are N-type
2 depletion mode MOSFETs.

1 6. The circuitry of claim 1 wherein the capacitors are
2 selected from the group consisting of on-chip metal
3 capacitors, on-chip poly capacitors, and discrete capacitors.

4 7. The circuitry of claim 1, wherein each of the capacitors
5 corresponds to a transmission gate switch.

1 8. The circuitry of claim 7, further comprising a set of
2 memory registers to provide the control signals for selecting
3 the individual capacitors

1 9. The circuitry of claim 8, wherein the transmission gate
2 switches are decoupled from the set of memory registers by a
3 set of buffer circuitry.

1 10. The circuitry of claim 9, wherein the set of buffer
2 circuitry is powered by a filtered power signal.

1 11. The circuitry of claim 1, wherein the oscillator includes
2 a resonator and an inverting amplifier.

1 12. The circuitry of claim 11, wherein a first subset of the
2 plurality of capacitors is selectively electrically coupled to
3 a first terminal of the resonator, and a second subset of the
4 plurality of capacitors is selectively electrically coupled to
5 a second terminal of the resonator

1 13 An electronic device comprising:
2 a real time clock for generating a system time signal,
3 the real time clock having a digitally tunable oscillator for

4 digitally adjusting an operating frequency of the real time
5 clock to speed up or slow down the system time signal; and
6 a memory device for storing data representing a
7 configuration of the digitally adjusted tunable oscillator.

1 14. The electronic device of claim 13, further comprising a
2 communication port for receiving a reference time signal,
3 wherein the digitally tunable oscillator is digitally adjusted
4 according to the reference time signal to minimize the
5 difference between the system time signal and the reference
6 time signal.

1 15. The electronic device of claim 13, wherein the digitally
2 tunable oscillator includes a capacitor bank having a set of
3 capacitors with capacitance values in a binary-weighted
4 relationship, the capacitors selectable through a set of
5 control signals.

1 16. A method comprising:
2 generating a set of control signals to select a subset of
3 capacitors from a set of capacitors;
4 connecting the selected subset of capacitors to an
5 oscillator;
6 generating an oscillating signal using the oscillator and
7 the selected subset of capacitors in combination; and

8 generating a system time signal using the oscillating
9 signal.

1 17. The method of claim 16, further comprising receiving a
2 reference time signal, comparing the reference time signal
3 with the system time signal, and modifying the set of control
4 signals in response to the difference between the reference
5 time signal and the system time signal to select a different
6 subset of capacitors.

7 18. The method of claim 17, further comprising saving data
8 representing the setting of the control signals in a memory.

1 19. A method of generating a time signal comprising:
2 generating a system time signal using a real time clock
3 circuit that has a tunable oscillator for adjusting an
4 operation frequency of the real time clock circuit;
5 receiving a reference time signal over a network;
6 adjusting the tunable oscillator to increase or decrease
7 the operating frequency of the real time clock circuit in
8 response to a difference between the system time signal and
9 the reference time signal.

1 20. The method of claim 19 wherein adjusting the tunable
2 oscillator comprises adjusting a set of control signals to

3 modify a selection of a set of capacitors within a capacitor
4 bank, the selection of the set of capacitors correlating to
5 the operating frequency of the real time clock circuit.

1 21. Apparatus for providing a variable level of capacitance,
2 comprising:

3 a plurality of capacitors, each capacitor selectable
4 through an independent control signal generated by a logic
5 circuit, the selected capacitors providing an amount of
6 capacitance that is the sum of the individual capacitances of
7 the selected capacitors; and

8 buffer circuitry for decoupling the plurality of
9 capacitors from the logic circuit to prevent noise in the
10 logic circuit from affecting the plurality of capacitors.

1 22. The apparatus of claim 21, further comprising a filter
2 circuit connected to a power supply to generate a filtered
3 power supply signal that is used to power the buffer
4 circuitry.

1 23. The circuit of claim 21, further comprising transmission
2 gates, each of which corresponds to one of the plurality of
3 capacitors and can be turned on by the independent control
4 signal when the corresponding capacitor is selected.

1 24. Apparatus comprising:

2 a control unit configured to generate a set of control
3 signals, each of which independently selects a capacitor from
4 a plurality of capacitors, the selected capacitors being
5 coupled to an oscillator, the selected capacitors in
6 combination providing a controllable amount of capacitance to
7 the oscillator to control the oscillating frequency of the
8 oscillator.

1 25. The apparatus of claim 24 in which the control unit is
2 disposed within a computer chipset.

1 26. The apparatus of claim 24, further comprising circuitry
2 for generating a system time signal based on the oscillating
3 frequency of the oscillator.

1 27. The apparatus of claim 26, further comprising a memory
2 for storing the configuration of the set of control signals,
3 and a data processing unit that processes data based on the
4 system time signal.